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Term	Documents
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L20	L18 and l7	21	L20
L19	L18 and l6	307	L19
L18	l11 and (simd or single near2 instruction$1)	590	L18
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L17	L16 and l15	12	L17
L16	(712/20-22)[CCLS]	404	L16
DB=PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR			
L15	(simd or single near2 instruction$1) and l12	133	L15
L14	L12 and l7	5	L14

L13	L12 and l6	88	L13
L12	L11 and endian$1	220	L12
L11	L10 and (align$8 or boundar$4)	21564	L11
L10	vector$1 near50 (size or length or width)	47079	L10

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L9	l5 and l7	5	L9
L8	l5 and l6	64	L8
L7	(711/201-221)[CCLS]	5460	L7
L6	(712/2-300)![CCLS]	11191	L6

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L5	L4 and (size or length or width)	136	L5
L4	L3 and (align$8)	139	L4
L3	L2 and endian$1	154	L3
L2	(load$4 or stor$4 or replicat$3 or written or writ$5) near15 vector$1 near12 register$1	4408	L2

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L1	5475823.pn.	1	L1

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Cheresiz, D.; Juurlink, B.; Vassiliadis, S.; Wijshoff, H.A.G.;
Very Large Scale Integration (VLSI) Systems, IEEE Transactions on
Volume 13, Issue 1, Jan. 2005 Page(s):1 - 13

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Verdier, C.; Boutillon, E.; Lafage, A.; Demeure, A.;
Application Specific Array Processors, 1994. Proceedings., International Conference on
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